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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,389	12/18/2001	Akihiko Ishibashi	60188-431	6491

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MCDERMOTT WILL & EMERY
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER
TRAN, MAI HUONG C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,389	ISHIBASHI ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *8-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

Applicant's election of Group II (claims 1-7 and 14-17) drawn to process of making a semiconductor device in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 and 14-17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,345,063 to Bour et al. in view of the remark.

Regarding to claim 1, Bour discloses a method for fabricating a semiconductor, comprising the steps of growing a first semiconductor layer made of $Al_xGa_{1-x}N$ 410 (0 <=

x <= 1) on a substrate 405 at a temperature higher than room temperature; and growing a second semiconductor layer made of $Al_uGa_vIn_wN$ 430 (0 <= u <= 1, 0 <= v <= 1, 0 <= w <= 1, u+v+w =1) over the first semiconductor layer 410 as set forth in col. 7, lines 19-67, fig. 5. Bour does not disclose the mole fraction x of Al of the first semiconductor layer is set so that the lattice constant of the first semiconductor layer at room temperature substantially matches with the lattice constant of the second semiconductor layer in the bulk state after thermal shrinkage or thermal expansion.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the mole fraction x of Al of the first semiconductor layer so that the lattice constant of the first semiconductor layer at room temperature substantially matches with the lattice constant of the second semiconductor layer in the bulk state after thermal shrinkage or thermal expansion since it was known in the art that the mole fraction x of Al of the first semiconductor layer is set so that the lattice constant of the first semiconductor layer at room temperature substantially matches with the lattice constant of the second semiconductor layer in the bulk state after thermal shrinkage or thermal expansion.

Regarding to claim 2, the method further comprising the step of growing a third semiconductor layer 440 having an Al mole fraction smaller than the second semiconductor layer between the first semiconductor layer and the second semiconductor layer or over the second semiconductor layer (col. 8, lines 1-12).

Regarding to claim 3, the method wherein the substrate is composed of sapphire, silicon carbide, or silicon (col. 7, lines 20-22).

Regarding to claim 4, Bour discloses a method for fabricating a semiconductor, comprising the step of growing a semiconductor layer made of $Al_uGa_vIn_wN$ 430 ($0 < u <= 1$, $0 <= v <= 1$, $0 <= w <= 1$, $u+v+w =1$) over a semiconductor substrate 405 made of $Al_xGa_{1-x}N$ ($0<=x<=1$) (col. 7, lines 19-21), wherein the lattice constant of the semiconductor substrate is made to substantially match with the lattice constant of the semiconductor layer in the bulk state (col. 7, lines 29-31, and col. 8, lines 1-12).

Regarding to claim 5, Bour discloses a method for fabricating a semiconductor, comprising the step of growing a semiconductor layer made of $Al_uGa_vIn_wN$ 430 ($0 < u <= 1$, $0 <= v <= 1$, $0 <= w <= 1$, $u+v+w =1$) over a semiconductor substrate 405 made of $Al_xGa_{1-x}N$ ($0<=x<=1$) (col. 7, lines 19-21).

Regarding to claim 6, the method wherein the semiconductor substrate contains indium (col. 7, lines 19-21).

Regarding to claim 7, Bour discloses a method for fabricating a semiconductor substrate 405, comprising the step of forming a semiconductor substrate 405 from $Al_xGa_{1-x}N$ ($0<=x<=1$) to be used as a substrate over which a semiconductor layer 430

made of $Al_uGa_vIn_wN$ 430 ($0 < u <= 1$, $0 <= v <= 1$, $0 <= w <= 1$, $u+v+w =1$) is grown. Bour does not disclose the mole fraction x of Al of the semiconductor substrate is set so that the lattice constant of the semiconductor substrate substantially matches with the lattice constant of the semiconductor layer in the bulk state.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the mole fraction x of Al of the semiconductor substrate so that the lattice constant of the semiconductor substrate substantially matches with the lattice constant of the semiconductor layer in the bulk state since it was known in the art that the mole fraction x of Al of the semiconductor substrate is set so that the lattice constant of the semiconductor substrate substantially matches with the lattice constant of the semiconductor layer in the bulk state.

Regarding to claims 14-17, Bour discloses the claimed invention except for the method wherein the first semiconductor layer is formed by supplying a material gas heated to a temperature of 1020°C.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the first semiconductor by supplying a material gas heated to a temperature of 1020°C, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (703) 305-1958. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mai-Huong Tran

David Nelms
Supervisory Patent Examiner
Technology Center 2800